IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants:	Jean-Yves SIMON, et al.	§	Confirmation No.:	9476
Serial No.:	10/764,670	§	Group Art Unit:	2112
Filed:	January 26, 2004	§	Examiner:	Fritz Alphonse
For:	Method for Streamlining Error Correction Code Computation While Reading or Programming a NAND Flash Memory	§	Docket No.:	TI-36989 (1962-09800)

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Date: June 26, 2009

Sir:

Appellants hereby submit this Appeal Brief in connection with the above-identified application. This Appeal Brief is filed in response to the Office Action of January 28, 2009, which is an Office Action issued after filing of a Notice of Appeal and Appeal Brief on October 29, 2008. Thus, the fee for the Appeal Brief has already been paid.

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I. REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Inc., a Delaware corporation, having its principal place of business in Dallas, Texas. The Assignment from the inventors to Texas Instruments was recorded on January 26, 2004, at Reel/Frame 014930/0563.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals or interferences.

III. STATUS OF THE CLAIMS

Originally filed claims:	1-26.
Claim cancellations:	None.
Added claims:	None.
Presently pending claims:	1-26.
Presently appealed claims:	1-26.

IV. STATUS OF THE AMENDMENTS

No claims were amended after the Office Action dated January 28, 2009.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The specification is directed to a method for streamlining Error Correction Code (ECC) computation while reading or programming a NAND flash memory. **{Specification Title}**.[1] At least some of the illustrative embodiments are methods as in claim 1:

1. A method, comprising:
   transferring a data block between a flash memory and a memory controller; **{12, [0033], lines 8-10, Figure 4a, element 408}**
   computing an ECC for said data block while transferring the data block; and **{12, [0033], lines 8-10, Figure 4a, element 408}**
   selectively storing the ECC in a plurality of registers using a switching mechanism, the storing while transferring the data block. **{12, [0033], lines 8-10, Figure 4a, element 408}**

Other embodiments are systems as in claim 6:

6. A system, comprising:
   a flash memory; **{3, [0016], lines 1-2, Figure 1a, element 114}**
   a controller coupled to the flash memory; **{3, [0016], lines 1-2, Figure 1a, element 100}**
   a switch coupled to the controller; and **{10, [0027], lines 2-4, Figure 1b, element 238}**
   said controller is configured to shift a data block between the flash memory and the controller, while computing an ECC for said data block; and **{11, [0030], lines 1-7, Figure 2, element 200}**
   said system is configured to selectively store the ECC in a plurality of registers using the switch, while the controller shifts the data block. **{11. [0030], lines 1-7, Figure 2, element 238}**

Yet still other embodiments are systems as in claim 12:

12. A system comprising:
   a means for storing[2] a data block; **{3, [0016], lines 1-2, Figure 1a, element 114}**
   a means for controlling[3] the data block; **{3, [0016], lines 1-2, Figure 1a, element 100}**

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[1] For consistency, citations to the Specification will take the form **{[page], [paragraph number], lines [lines within the paragraph]}.**

[2] This limitation is specifically identified as a Means plus Function under 35 U.S.C § 112, 6th.

[3] This limitation is specifically identified as a Means plus Function under 35 U.S.C § 112, 6th.

a means for computing[4] an ECC of the data block; **{11, [0030], lines 3-6, Figure 2, element 202}**
a means for shifting[5] the data block between the means for storing and the means for controlling while computing an ECC for said data block; and **{11, [0030], lines 1-7, Figure 2, element 200}**
a means for selectively storing[6] the ECC in a plurality of registers while shifting the data block. **{11, [0030], lines 1-7, Figure 2, element 238}**

Other embodiments are memory controllers as in claim 18:

18. A memory controller configured to couple to a memory, comprising:
a memory interface; **{10, [0027], lines 5-8, Figure 2, element 204}**
an ECC engine configured to compute an ECC while transferring a data block between the ECC engine and memory; and **{11, [0030], lines 3-6, Figure 2, element 202}**
a switching mechanism coupled to the ECC engine, the ECC engine configured to selectively store the ECC in a plurality of registers using the switching mechanism, while transferring the data block. **{11, [0030], lines 1-7, Figure 2, element 238}**

[4] This limitation is specifically identified as a Means plus Function under 35 U.S.C § 112, 6th.

[5] This limitation is specifically identified as a Means plus Function under 35 U.S.C § 112, 6th.

[6] This limitation is specifically identified as a Means plus Function under 35 U.S.C § 112, 6th.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1, 6, 12 and 18-19 are obvious under 35 U.S.C. §103(a) over Tamada et al. (US Pat. No. 6,353,553, hereinafter 'Tamada'), in view of Hsu et al. (US PGPub No. 2005/0111567, hereinafter 'Hsu').

Whether claims 2-4, 7-10, 13-16 and 20-26 are obvious under 35 U.S.C. §103(a) over Tamada, Hsu and Eggleston et al. (US Pat. No. 9,906,961, hereinafter 'Eggleston').

Whether claims 5, 11 and 17 are obvious under 35 U.S.C. §103(a) over Tamad, Hsu and Acton (US Pat. No. 6,883,131, hereinafter 'Acton').

VII. ARGUMENT

A. Section 103 Rejections over Tamada and Hsu

1. Claims 1-4, 6-10 and 18-26

Claims 1, 6, 12 and 18-19 stand rejected as allegedly obvious over Tamada and Hsu. Claim 1 is representative of this grouping of claims. The grouping should not be construed to mean the patentability of any of the claims may be determined in later actions (*e.g.*, actions before a court) based on the groupings. Rather, the presumption of 35 USC § 282 shall apply to each of these claims individually.

Tamada is directed to a data storage comprising a nonvolatile semiconductor memory device having structure storing multivalued data.[7] In particular, Tamada teaches a data storage system comprising a binary flash memory, a plurality of multivalued flash memories and a system controller including a timer, buffer and an error correction circuit.[8] The buffer captures data transferred from a host system to flash memories in the data storage system, and the buffer captures data read from the flash memories in the data storage system to the host system.[9] Tamada also teaches performing error correction coding after the data read from the flash memory has been transferred to the controller. Tamada's Figure 34 is reproduced immediately below for convenience of the discussion.

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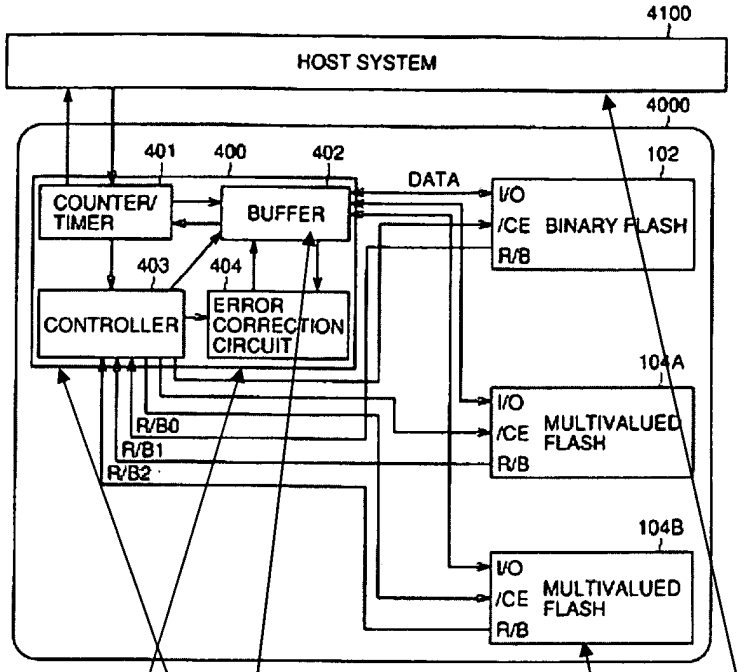
[7] Tamada Title.

[8] Tamada Col. 17, lines 31-37.

[9] Tamada Col. 17, lines 65-67.

FIG.34



When receiving a read request form the host system 4100 (step S450), the system controller 400 transfers corresponding data stored in any flash memory to the buffer 402 (step S451).

The system controller 400 determines whether or not the data transferred to the buffer 402 is read from any multivalued flash memory (step S452).

...

If the data is read from the multivalued flash memory, the system controller 400 transmits the data transferred to the buffer 402 to the error correction circuit 404 (step S453). The error correction circuit 404 executes error correction (step S454). The buffer 402 stores the data subjected to error correction (step S455). Then the process shifts to the processing of transferring the data from the buffer 402 to the host system 4100 (step S456).[10]

Accordingly, Tamada appears to teach transferring data from the flash memory to a buffer within the controller, and thereafter performing error correction if the data is from a multivalued flash memory.

[10] Tamada Col. 20, lines 23-44.

Representative claim 1, by contrast, specifically recites "transferring a data block between a flash memory and a memory controller; computing an ECC for said data block while transferring the data block." Appellants submit that Tamada and Hsu do not teach or fairly suggest such a method. Tamada teaches that first the data from the flash memories is transferred to the buffer in controller. Second, the controller determines whether the data transferred to the buffer is from multivalued flash. Finally, if the data is from the multivalued flash, error correction is performed on the data in the buffer. Stated otherwise, Tamada teaches performing error correction after the data has been transferred to the controller. Thus, even if the teachings of Hsu are precisely as the Office Action suggests (which Appellants do not admit), Tamada and Hsu still fail to teach or fairly suggest "transferring a data block between a flash memory and a memory controller; **computing an ECC for said data block while transferring the data block**."

Hsu is directed to adaptive data transmitter having rewriteable non-volatile storage.[11] In particular, Hsu teaches a finite impulse response (FIR) transmitter, and a flash memory that provides a rewriteable non-volatile storage operable to store values of coefficients used in the taps of the FIR transmitter.[12] The flash memory includes a flash memory array, a column switch, and a shift register.[13] Hsu also teaches that the shift register holds data for transfer between the flash memory array and the FIR transmitter.

> Operation of the flash memory 20 proceeds as follows. When an address is received from the controller 10, a write operation is performed to the flash memory array 203. Data is then inputted serially into the shift register 205 from signal Data_in, where it is then available to be subsequently stored to the flash memory array 203. When read control input is received, the information stored in the flash memory array is read out to the shift register through the column switch 204. From the shift register 205, the retrieved information is then available for output to the FIR transmitter 30 or be outputted serially as Data_out, for a test purpose, for example.[14]

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[11] Hsu Title.

[12] Hsu Paragraph [0019].

[13] Hsu Paragraph [0023].

[14] Hsu Paragraph [0028].

Thus, Hsu teaches a single shift register to transfer data between flash memory and a FIR transmitter.

Representative claim 1, by contrast, specifically recites "selectively storing the ECC in a plurality of registers using a switching mechanism, the storing while transferring the data block." Appellants submit that Tamada and Hsu do not teach or fairly suggest such a method. Appellants respectfully submit that Hsu does not teach calculating ECC for the data transmitted between flash memory and a controller. Moreover, Hsu does not teach storing the ECC in a plurality of registers using a switching mechanism. Hsu merely teaches a single shift register to transfer data between flash memory and a FIR transmitter. Thus, Tamada and Hsu still fail to teach or fairly suggest "**selectively storing the ECC in a plurality of registers using a switching mechanism**, the storing while transferring the data block."

Based on the foregoing, Appellants respectfully request that the rejection of this grouping be reversed, and the claims set for issue.

B. Section 103 Rejections over Tamada, Hsu and Eggleston

1. Claims 2-4, 7-10, 13-16 and 20-26

Claims 2-4, 7-10, 13-16 and 20-26 stand rejected as allegedly obvious over Tamada, Hsu and Eggleston. Claims 2-4, 7-10, 13-16 and 20-26 are allowable for at least the same reasons as delineated in Sections VII(A)(1).

C. Section 103 Rejections over Tamada, Hsu and Acton

1. Claims 5, 11 and 17

Claims 5, 11 and 17 stand rejected as allegedly obvious over Tamada, Hsu and Acton. Claims 5, 11 and 17 are allowable for at least the same reasons as delineated in Sections VII(A)(1).

D. Conclusion

For the reasons stated above, Appellants respectfully submit that the Examiner erred in rejecting all pending claims. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to the Texas Instruments, Inc. Deposit Account No. 20-0668.

Respectfully submitted,

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VIII. CLAIMS APPENDIX

1. (Previously Presented) A method, comprising:

transferring a data block between a flash memory and a memory controller;

computing an ECC for said data block while transferring the data block; and

selectively storing the ECC in a plurality of registers using a switching mechanism, the storing while transferring the data block.

2. (Original) The method of claim 1, wherein transferring the data block comprises transferring the data block between a NAND Flash memory and the memory controller.

3. (Previously Presented) The method of claim 1, wherein selectively storing the ECC further comprises

storing a first portion of the ECC in a first register; and

storing a second portion of the ECC in a second register if the first register is full.

4. (Previously Presented) The method of claim 3, wherein storing in a second register comprises selecting the second register using the switching mechanism.

5. (Original) The method of claim 1, wherein computing the ECC comprises performing the exclusive-or function.

6. (Previously Presented) A system, comprising:

a flash memory;

a controller coupled to the flash memory;

a switch coupled to the controller; and

said controller is configured to shift a data block between the flash memory and the controller, while computing an ECC for said data block; and

said system is configured to selectively store the ECC in a plurality of registers using the switch, while the controller shifts the data block.

7. (Original) The system of claim 6, wherein the flash memory is a NAND Flash memory.

8. (Previously Presented) The system of claim 6, wherein the system is configured to
store a first portion of the ECC in a first register; and
store a second portion of the ECC in an alternate register if the first register is full.

9. (Previously Presented) The system of claim 8, wherein the controller is configured to transfer contents of all registers to memory if all registers are full.

10. (Previously Presented) The system of claim 8, wherein the switch configured to select the alternate register.

11. (Previously Presented) The system of claim 6, wherein the controller is configured to compute the ECC while performing the exclusive-or function.

12. (Previously Presented) A system comprising:
a means for storing a data block;
a means for controlling the data block;
a means for computing an ECC of the data block;
a means for shifting the data block between the means for storing and the means for controlling while computing an ECC for said data block; and
a means for selectively storing the ECC in a plurality of registers while shifting the data block.

13. (Original) The system of claim 12, wherein the means for storing is a NAND Flash memory.

14. (Previously Presented) The system of claim 12, wherein the means for selectively storing the ECC is configured to

store the ECC in a first register; and

store the ECC in an alternate register if the first register is full.

15. (Previously Presented) The system of claim 12, wherein the system is configured to transfer contents of at least one register to memory if all registers are full.

16. (Previously Presented) The system of claim 14, wherein the means for selectively storing the ECC is a switch configured to select the alternate register.

17. (Previously Presented) The system of claim 12, wherein the system is configured to compute the ECC while performing the exclusive-or function.

18. (Previously Presented) A memory controller configured to couple to a memory, comprising:

a memory interface;

an ECC engine configured to compute an ECC while transferring a data block between the ECC engine and memory; and

a switching mechanism coupled to the ECC engine, the ECC engine configured to selectively store the ECC in a plurality of registers using the switching mechanism, while transferring the data block.

19. (Previously Presented) The memory controller of claim 18, further comprising:

a register bank coupled to the switching mechanism, comprising at least one register;

wherein the ECC engine configured to store the ECC in a register selected by the switching mechanism, the register having space available for ECC storage.

20. (Previously Presented) The memory controller of claim 18, wherein the controller is configured to transfer a data block while transferring the data block between the ECC engine and a flash memory.

21. (Previously Presented) The memory controller of claim 18, wherein the controller is configured to transfer a data block while transferring the data block between the ECC engine and a NAND Flash memory.

22. (Previously Presented) The memory controller of claim 18, wherein the ECC engine is configured to transfer a data block by reading the data block from memory.

23. (Previously Presented) The memory controller of claim 18, wherein the ECC engine is configured to transfer a data block by writing the data block to memory.

24. (Previously Presented) The system of claim 8, wherein the first register is in the controller.

25. (Previously Presented) The system of claim 8, wherein the alternate register is in the controller.

26. (Previously Presented) The system of claim 10, wherein the switch is in the controller.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.